TTM Syracuse Wireless (SYR-W)
a member of TTM Technologies Group
5823 Widewaters Parkway
East Syracuse, NY, 13057
Tel 315.233.5510
www.ttm.com

ANN-8804 REV B.

POWER HANDLING CONSIDERATIONS FOR SMD TERMINATIONS, ATTENUATORS AND RESISTORS

This document describes the power rating of high power surface mount resistive products. Furthermore, techniques for maximizing power handling performance of these parts are detailed.

SMD POWER RATING AND DERATING:

TTM Wireless provides power ratings for all SMD resistive components. This power rating is based on the temperature at the solder interface, where the solder is in contact with the SMD component (see Figures 1a and 1b). This solder interface temperature is 100°C. This means that if the solder temperature is maintained at 100°C, then the part may safely operate at the specified power rating. If the solder interface temperature is greater than 100°C, then the operating power must be decreased proportionally according to the part's derating curve. TTM Wireless datasheet power derating curves assume use of SAC solder. If another type of solder is use, the proportional decrease in power will differ (see Figure 2).

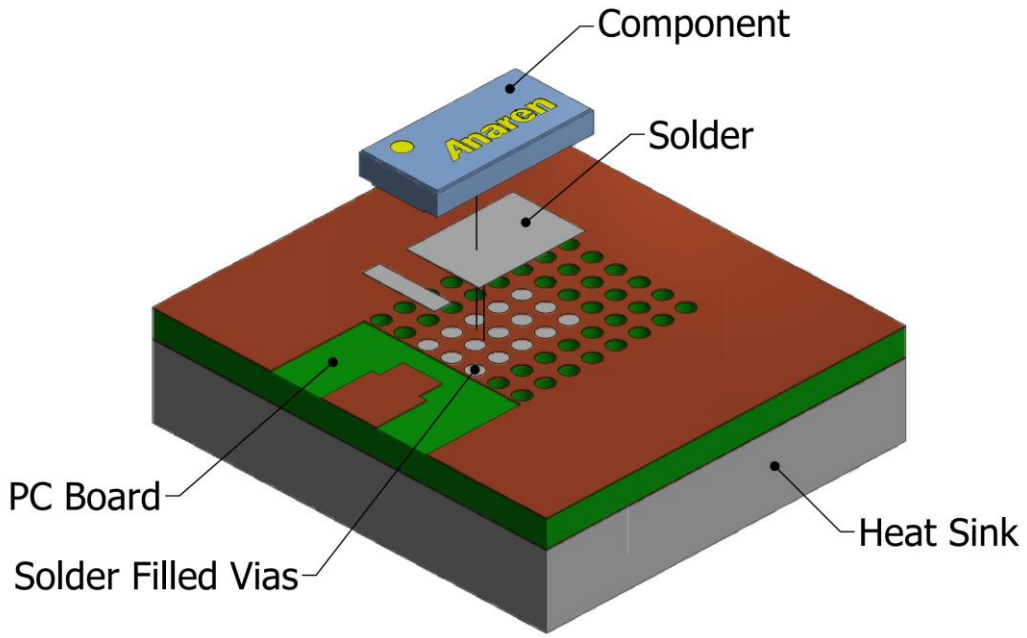


Figure 1a: 3-D view of a typical stackup and layout for SMD component.

TTM Technologies
Time-To-Market Interconnect Solutions

TTM Syracuse Wireless (SYR-W)
a member of TTM Technologies Group
5823 Widewaters Parkway
East Syracuse, NY, 13057
Tel 315.233.5510
www.ttm.com

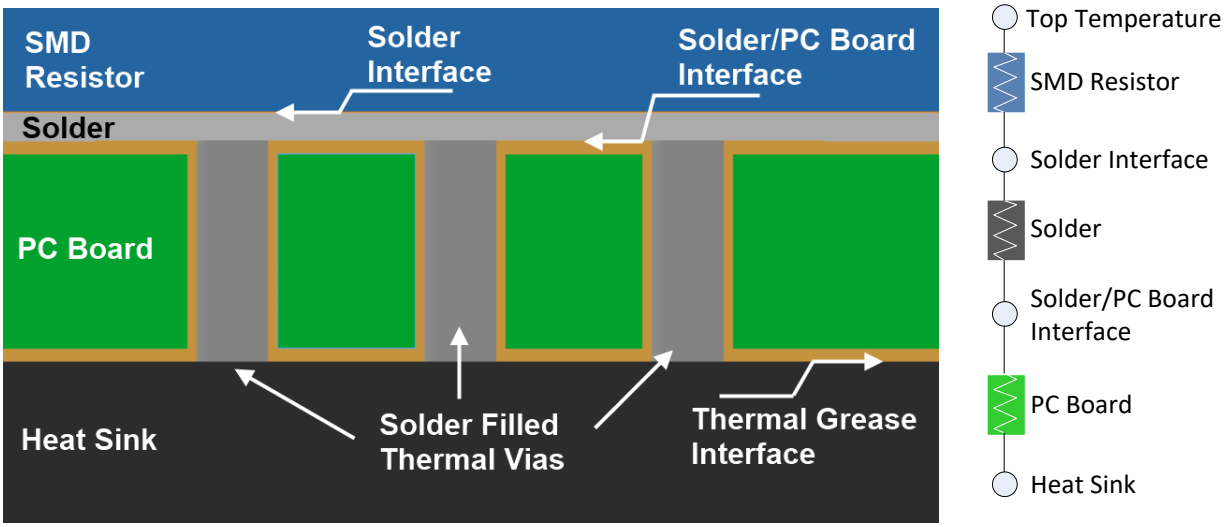


Figure 1b: 2-D cross section view of a typical stackup and layout for SMD component and corresponding thermal path.

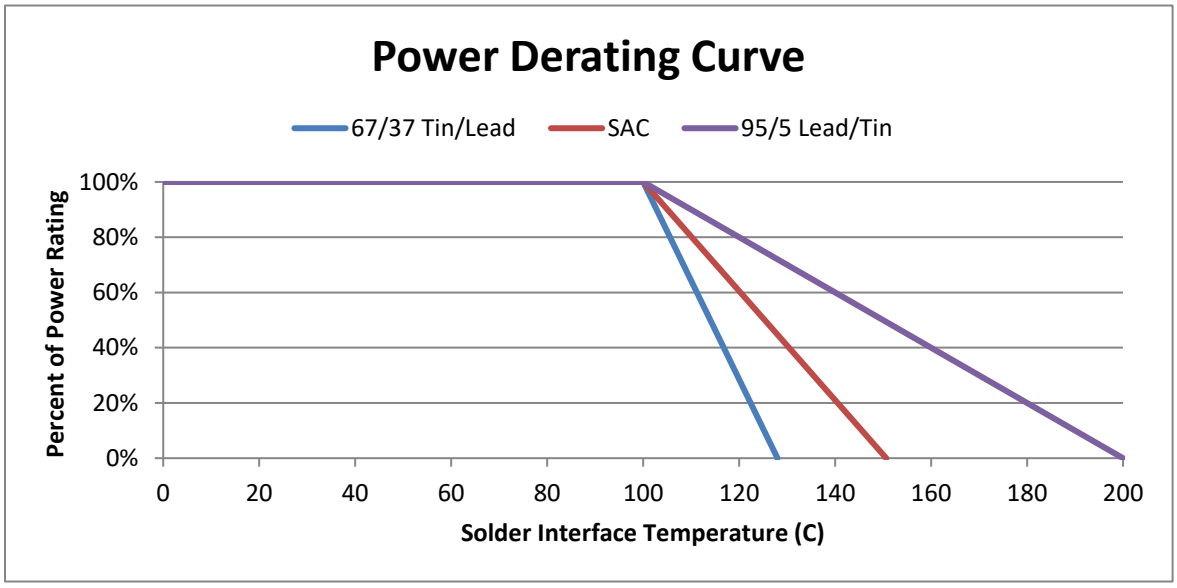


Figure 2: Power derating as a result of increased solder interface temperature.

The power handling performance of the parts is affected by the design of the Printed Circuit Board to which it is attached, and the assembly processes. The following sections describe the effects these aspects have on power handling performance and how they can be optimized.

TTM Technologies
Time-To-Market Interconnect Solutions

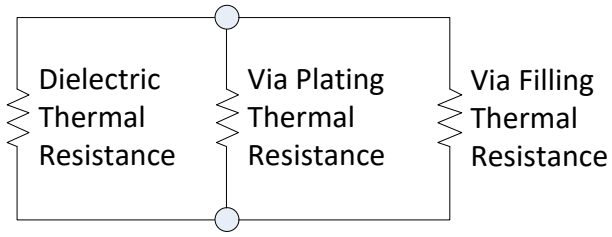
TTM Syracuse Wireless (SYR-W)
a member of TTM Technologies Group
5823 Widewaters Parkway
East Syracuse, NY, 13057
Tel 315.233.5510
www.ttm.com

PRINTED CIRCUIT BOARD DESIGN

In the system described in Figures 1a and 1b, the PCB will have the highest thermal resistance and the board design will have the most significant impact on the power handling of the system. It is very important to reduce the thermal resistance of the PC board as much as possible.

The total thermal resistance of the PCB is the reciprocal sum of the thermal resistances of the dielectric, the via plating, and the via fill (see equation and circuit diagram below).

$$\frac{1}{\theta_{pcb}} = \frac{1}{\theta_d} + \frac{1}{\theta_{vp}} + \frac{1}{\theta_{vf}}$$



where:

- θ_{pcb}: total PCB thermal resistance
- θ_d: dielectric thermal resistance
- θ_{vp}: via plating thermal resistance
- θ_{vf}: via filling thermal resistance.

Each thermal resistance in the above equation is a result of thermal conductivity. Other forms of heat transfer (convection and radiation) will not significantly contribute. To calculate the thermal resistance due to thermal conductivity, the following equation is used:

$$\theta = \frac{L}{kA}$$

where:

- θ: thermal resistance
- L: length through which heat must travel
- k: thermal conductivity of the material
- A: area of the cross section through which heat must travel.

In order for a PCB to dissipate heat from the device at the specified power rating and solder interface temperature, the PCB must be designed with a low thermal resistance. According to the following equation, change in temperature is equal to thermal resistance multiplied by dissipated power.

$$\Delta T = \theta * Q \quad \text{or} \quad T_1 - T_2 = \theta * Q$$

where:

- θ: thermal resistance
- ΔT: change in temperature
- T_1: solder interface temperature
- T_2: test board bottom temperature
- Q: dissipated heat

If thermal resistance is too high, T_2 will need to be very low, which may not be practical. It is recommended to keep ΔT below 50°C. As Q increases, θ must decrease to maintain a small ΔT. For example, If T_1 = 100°C, T_2= 50°C,

TTM Technologies
Time-To-Market Interconnect Solutions

TTM Syracuse Wireless (SYR-W)
a member of TTM Technologies Group
5823 Widewaters Parkway
East Syracuse, NY, 13057
Tel 315.233.5510
www.ttm.com

and Q=10W, θ should be 5°C/W or lower. The table below shows suggested test board thermal resistance values for various dissipated power values.

Q (W)	10	20	30	50	100	200
R (°C/W)	ΔT					
0.01	0.1	0.2	0.3	0.5	1	2
0.05	0.5	1	1.5	2.5	5	10
0.10	1	2	3	5	10	20
0.20	2	4	6	10	20	40
0.30	3	6	9	15	30	60
0.40	4	8	12	20	40	80
0.50	5	10	15	25	50	100
1.00	10	20	30	50	100	200
1.50	15	30	45	75	150	300
2.00	20	40	60	100	200	400
2.50	25	50	75	125	250	500
3.00	30	60	90	150	300	600
4.00	40	80	120	200	400	800
5.00	50	100	150	250	500	1000
10.00	100	200	300	500	1000	2000
15.00	150	300	450	750	1500	3000
20.00	200	400	600	1000	2000	4000
25.00	250	500	750	1250	2500	5000

Table 1

The thermal resistance of the PCB is affected by:

- The quantity of vias
- The via diameter
- The copper plating thickness in the vias
- The PCB height
- Via fill

In all cases, increasing the copper plating thickness or decreasing the PCB height will decrease the thermal resistance of the thermal vias.

THERMAL VIA DIAMETER

Increasing the cross sectional area of the thermal vias will decrease the thermal resistance because the copper and solder have higher thermal conductivity than the PCB material. However, the number of thermal vias that can fit underneath the ground pad is dependent on via diameter and spacing. In most cases, reducing the via diameter to allow more vias to fit in the area will improve the thermal resistance. Consider a PCB with all vias solder filled and a 0.100" by 0.200" rectangular ground pad (assume 1mil plating thickness). The table below shows the number of vias that can fit, the center to center spacing, the cross sectional area of those vias, and the resulting thermal resistance of the PCB when varying the via diameter.

***Note**: The table below describes the use of a four point layout (see Page 6 for information about alternative three point layout).*

TTM Syracuse Wireless (SYR-W)
a member of TTM Technologies Group
5823 Widewaters Parkway
East Syracuse, NY, 13057
Tel 315.233.5510
www.ttm.com

Via Diameter	Number of Vias	Spacing Center to Center (between via wall)	Via Drill cross sectional area (in^2)	Via cross sectional area (in^2)	Thermal Resistance (°C/W) w/Solder Fill	Thermal Resistance (°C/W) w/No Fill
0.006”	162	11mil (5mil)	0.0046	0.0025	1.19	1.33
0.008”	120	13mil (5mil)	0.0060	0.0026	1.08	1.28
0.010"	91	15mil (5mil)	0.0071	0.0026	1.05	1.32
0.015"	50	20mil (5mil)	0.0088	0.0022	1.07	1.54
0.020"	32	25mil (5mil)	0.0101	0.0019	1.10	1.78
0.025"	18	30mil (5mil)	0.0088	0.0014	1.39	2.48
0.030"	15	35mil (5mil)	0.0106	0.0014	1.25	2.47
0.035"	10	40mil (5mil)	0.0096	0.0011	1.47	3.15
0.040"	8	45mil (5mil)	0.0101	0.0010	1.48	3.43

Table 2

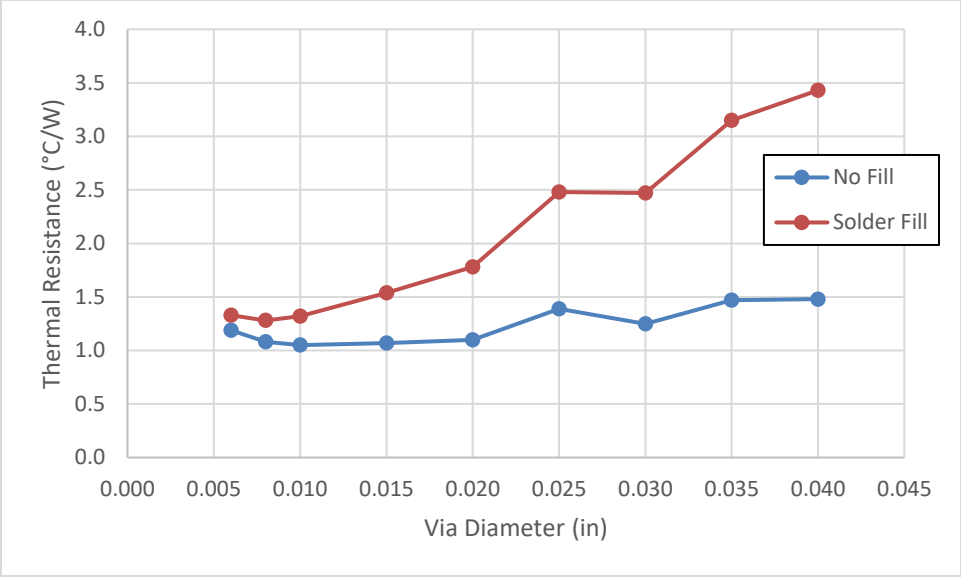


Figure 3: Thermal resistance of thermal vias with respect to the via diameter.

A smaller diameter yields more vias and in general will yield a lower thermal resistance. This effect has a bigger impact when there is no fill in the vias.

THERMAL VIA QUANTITY:

While via quantity is typically constrained by manufacturing limits on diameter and spacing, alternative layouts may allow more vias to fit in the area allotted. There are two layouts that maximize the number of vias: three point layout and four point layout (see Figure 4). If the three point layout can provide additional thermal vias, then it should be used. For example, in Figure 4, the four point layout provides 30 thermal vias while the three point layout provides 32 thermal vias of the same diameter in the same area.

TTM Syracuse Wireless (SYR-W)
a member of TTM Technologies Group
5823 Widewaters Parkway
East Syracuse, NY, 13057
Tel 315.233.5510
www.ttm.com

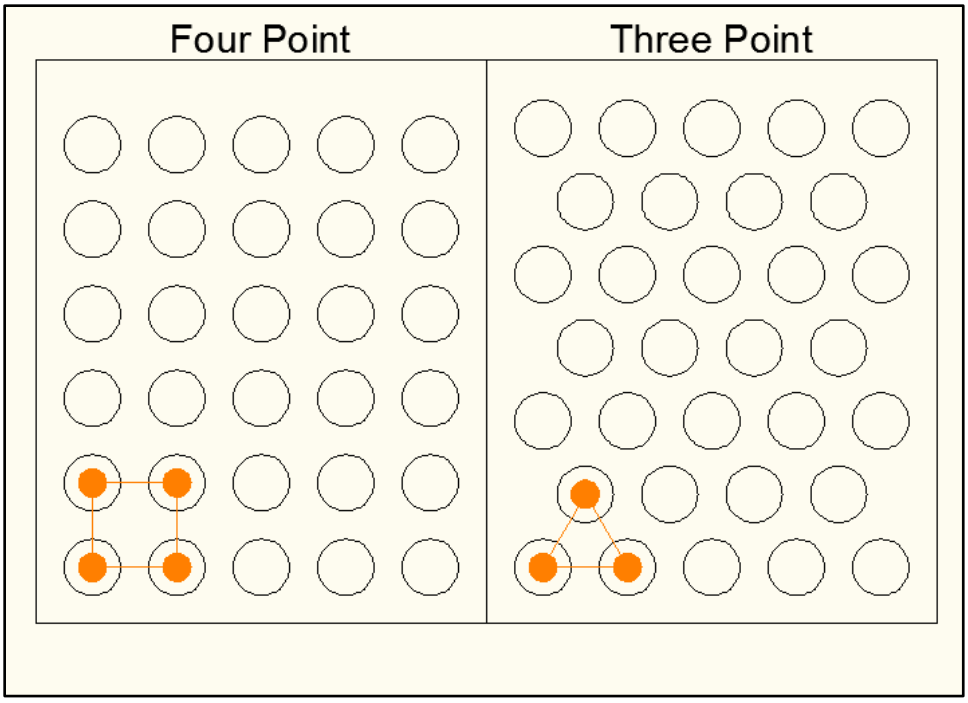


Figure 4: The two most common thermal via layout patterns.

THERMAL VIA FILL

Typical test board thermal vias have no fill but ensuring that all thermal vias are solder filled can significantly reduce the overall thermal resistance of the PCB. Typical SAC solder has a thermal conductivity of 57 $^{W}/_{m\text{-}K}$ and it is recommended that all thermal vias be filled with solder.

Other fill materials include epoxy via fill material and copper. If it is feasible, filling vias with copper will decrease thermal resistance by a large factor. Most via fill pastes have low thermal conductivity and in most cases it is better to have only some vias filled with solder than to have all vias filled with via fill paste.

For example, if we consider a single via of 0.035" diameter and with 0.001" thick copper plating in a PCB area of 0.010 in^2 (0.1”x 0.1”), the resulting thermal resistances are provided in the following table:

Situation	**Thermal Resistance**
No solder fill (air fill)	27.8 $^{\circ C}/_{W}$
Via Fill Paste	27.6 $^{\circ C}/_{W}$
Solder fill	13.8 $^{\circ C}/_{W}$
Copper fill	3.5 $^{\circ C}/_{W}$

Table 3

TTM Technologies
Time-To-Market Interconnect Solutions

TTM Syracuse Wireless (SYR-W)
a member of TTM Technologies Group
5823 Widewaters Parkway
East Syracuse, NY, 13057
Tel 315.233.5510
www.ttm.com

COPPER COIN

As seen above, copper filled vias provide an excellent thermal path in a PCB. As vias spacing decreases and vias get closer together, the via pattern starts to resemble a copper coin or flange. This is best possible thermal path under a device. Referring back to Table 1, a copper coin will minimize change in temperature across the board and offer the most efficient thermal path for dissipating heat generated by the component.

Situation	**Thermal Resistance**
No solder fill (air fill)	27.8 $^{\circ C}/_{W}$
Copper coin	0.34 $^{\circ C}/_{W}$

Table 4

SOLDER JOINT QUALITY

All of the power dissipated in the SMD component must pass through solder before reaching the heat sink. A poor quality solder joint could reduce the power handling capability of the part. It is important to maintain solder joints that are 0.002" to 0.003" in height and have 20% or lower, void percentage. See Application Note ANN-8803 for more information.

CONCLUSION

The power handling value provided by TTM Wireless for all SMD resistive components is the input power at which the component can be safely operated, when the solder interface temperature is maintained at 100°C or lower. However, in a typical design, heat dissipation and the temperature at the solder interface is affected by the PCB design. Thus, TTM Wireless makes the following recommendations when designing a low thermal resistance PCB for mounting SMD terminations, attenuators and resistors:

- Minimize the thickness of the PCB
- Maximize the cross sectional area of thermal vias underneath the ground pad of the SMD component.
- Ensure good quality solder joints that are 0.002” to 0.003” in height and have 20% or less, solder void percentage.
- Maximize the number of thermal vias under the ground pad by utilizing the three point layout (in some situations, both the three and four point layouts will yield the same number of vias. In those situations, it does not matter which layout is chosen).
- Where necessary, use a copper coin for improved thermal path and minimized thermal resistance.

Customers must use simulation and empirical testing to validate their particular systems.