

ANN-8801 REV A.

THERMAL POWER TESTING METHODOLOGY FOR CHIP, FLANGE, AND SMD (PCB MOUNTED) RESISTIVE COMPONENTS

In the global electronics market, resistive components (resistors, attenuators, and terminations) are used in a variety of applications and deployed to handle a many different duties ranging from dissipating excess power, to providing a system safety mechanism, to providing a matching device, among other tasks.

A resistor operates by converting electrical energy into heat energy by means of a resistive element. In most applications, resistive components are mounted to a heatsink, a flange (as depicted in Figure 1 and Figure 2), or directly on a PCB using industry-standard solders. When DC or RF power is input into the resistive component, the power is converted by the resistive element into heat. In the case of a flange-mounted component, heat flows from the element into the ceramic dielectric material and the solder joint, through the flange and into the heatsink.

Typically, there are two main design considerations for validating a resistive component chip design:

- **Temperatures/heat generated in the application and the effect this heat has on the resistive component's materials:** High temperatures may exceed the limitations of the materials used in a resistive component (causing reliability issues). Moreover, excessive temperatures sustained for a duration of time can even result in permanent damage or complete failure of the resistive component.
- **Coefficient of Thermal Expansion (CTE) mismatches between the resistive component's materials:** When power is dissipated in a resistive component, a temperature gradient through the ceramic, solder, flange (or PCB), heatsink results. The temperature gradient, along with the CTE mismatch of the materials, creates stress. The solder joint (Figure 2) is subject to fatigue cracking due to repeated exposure to this stress. A robust design is required to ensure that, as the resistive component is cycled on and off over time, its materials will not fatigue and degrade and eventually lead to failure.

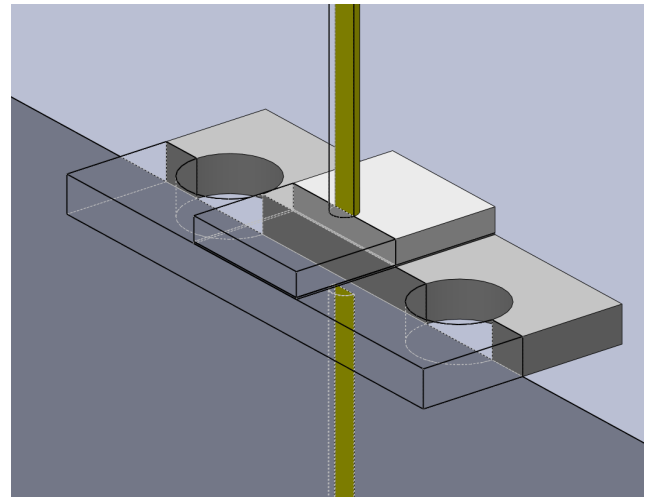


Figure 1: CROSS-SECTIONAL VIEW OF TEST SETUP

The materials used in TTM resistive components are selected to minimize the Coefficient of Thermal Expansion (CTE) mismatch and reduce stress. To accomplish this, TTM has developed a test method that ensures that the design is robust, meets the desired power handling requirements, and performs consistently and reliably for the design life of the resistive component. More specifically, a customized test station is utilized to determine and validate a resistive component's power handling capabilities and design. This test station has the ability to finely

control the interface temperature (see Figure 2) during testing, allowing for accurate, reliable test data and analysis.

As seen in Figure 1 and Figure 2, the resistive component is soldered to a flange or PCB and then mounted to the test station's heat sink. Thermocouples and an IR camera are used to monitor and collect temperature data during the testing. The Film Thermocouple or IR camera monitors the resistive element's temperature. The Interface Thermocouple is mounted adjacent to the part, as close as possible to the ground pad and monitors the interface temperature.

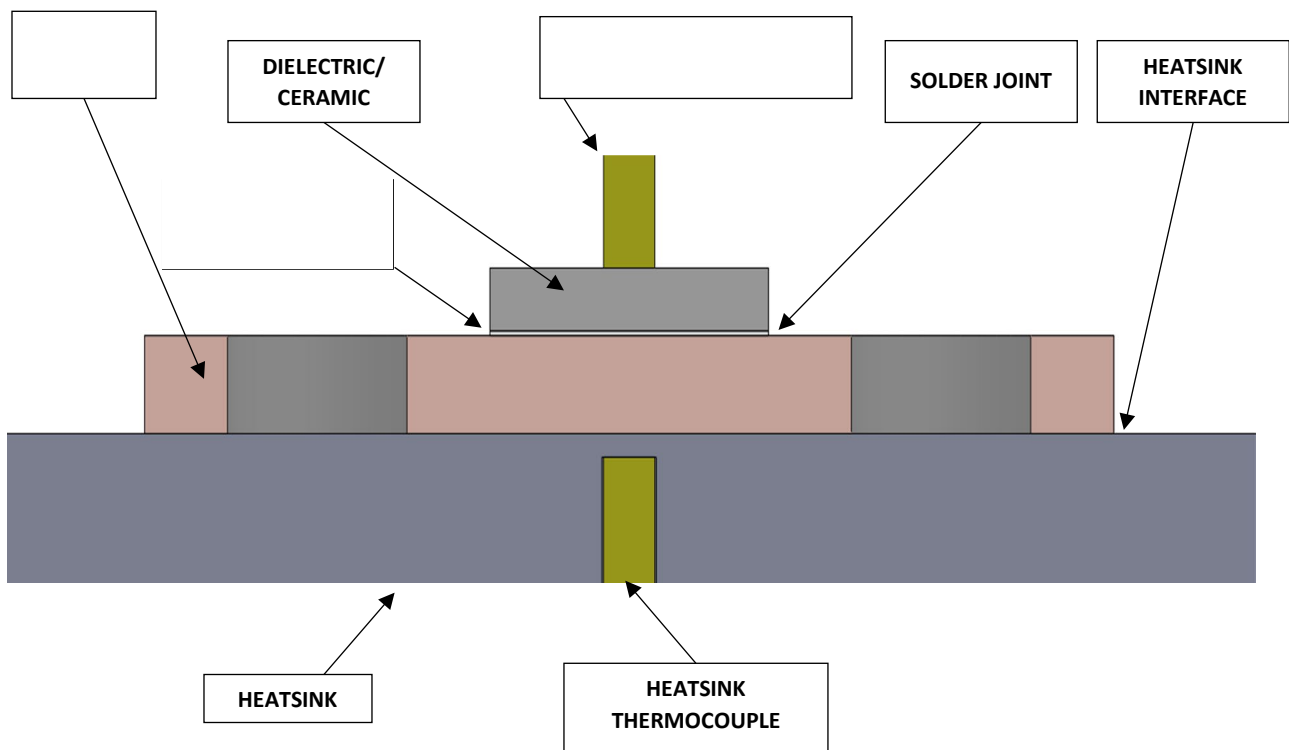


FIGURE 2: CROSS-SECTIONAL SIDE VIEW OF TEST SETUP

Testing is performed in two (2) phases. Phase 1 verifies that the resistive component design will handle the intended maximum input power. This phase of testing subjects the resistive component to the intended maximum input power while maintaining a 100C interface temperature (refer to Figure 3 – “Test Point”). The resistive film temperature is monitored to verify that maximum operating temperature boundary limits are not exceeded. If the resistive component stays within the set temperature boundary range, and if there is no damage to the resistive element, the chip is subjected to the second phase of testing.

Once the chip’s power handling capability is verified by the first phase of the testing, it is subjected to the second phase of testing designed to verify the long term reliability. Phase 2 testing subjects the resistive component to cyclic thermal/power levels to verify that the unit can survive the stress resulting from CTE mismatches; a typical profile for the test method is shown in Figure 4.

The resistive element/film temperature is monitored during the test. At the conclusion of the test, the entire resistive component is analyzed to ensure it was not damaged. On the start of a cycle, the system and the device under test (DUT – in this case, the resistive component soldered to the flange/PCB) is at room temperature (25°C). Full input power is applied to the chip and the interface temperature (or “Flange Temperature” as depicted in Figure 4) is brought to and maintained at 100°C. Once the flange/interface temperature stabilizes (at 100°C), the chip is pulsed 10 cycles of ‘power on – power off’; essentially, the pulsing consists of full power applied for 3 seconds proceeded by no power for 3 seconds. At the completion of 10 cycles, power to the chip is turned off and the entire system (heatsink and DUT) is cooled back down to room temperature. This process is repeated 300 times for a total of 3,000 pulses.

Once testing is complete, a post examination of the chip is performed to ensure that there is no permanent damage or change due to testing; a permanent change in resistance indicates that the chip is at risk for unreliable performance over the design life. Additionally, this two phase testing process is completed on multiple samples to ensure confidence in the data accuracy and ultimately the reliability of the resistive component.

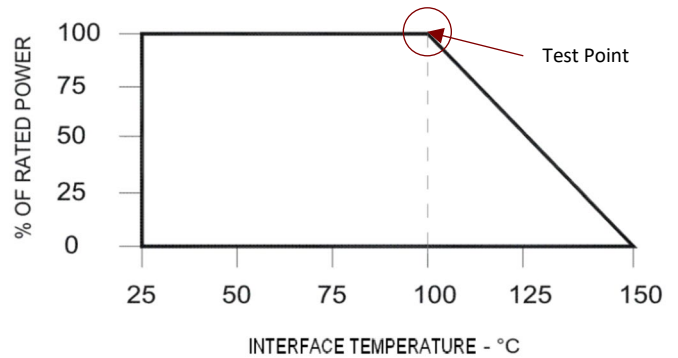


FIGURE 3: TYPICAL DERATING CURVE FOR INPUT POWER

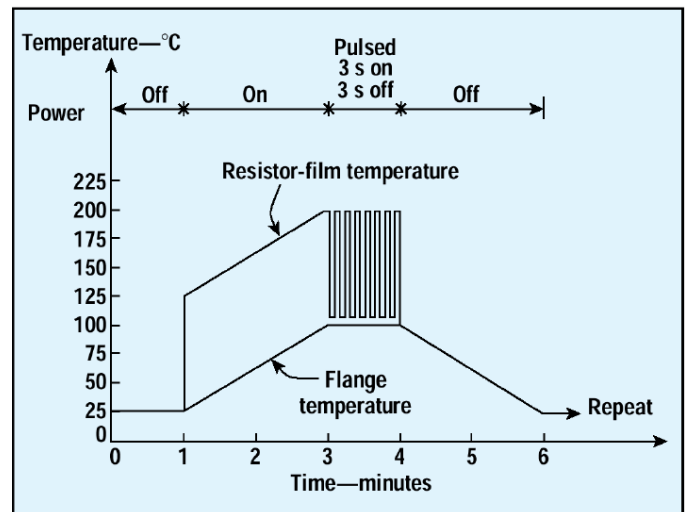


Figure 4: PHASE TWO TEST PROFILE FOR CTE MISMATCH